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VLSI Architecture of APT-VDF Using Novel RTSD Adder and Modified Booth Multiplier

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Abstract*— Variable digital filters are the most important element in communication and signal processing. The important requirement of APT-VDF design is speed optimization and area. This paper focus on the design of proposed modified pipeline APT-VDF from an arithmetic perception. So the addition & multiplication are the basic arithmetic operations used to define the convolution equations. For multiplication, modified Booth encoding is utilized in order to reduce the number of partial products. Therefore for improving addition speed, consider carry-propagation free addition approaches. The method used to enhance speed of addition utilized in this work is redundant ternary signed-digit (RTSD) number framework. The redundant ternary illustration uses number of bits than the single binary digit. Exceptional behaviour of RTSD supports the calculation along with the lack of classic carry propagation. Finally, the FIR filter is designed by using APT-VDF technique. From the implementation result, the proposed design of APT-VDF achieves 799 flip flops, 850 slices, 38 IOB's, 325.119(MHz) operating frequency, 3.769(W) power consumption and 3.076 (ns) latency.

Index Terms*— APT based VDF, Redundant Ternary Signed –Digit (RTSD) adder, Modified booth multiplier, Finite Impulse Response (FIR) filter, power and delay.

1. INTRODUCTION

The filters are used to the purpose of eliminating the signals undesirable portions on signal processing such as, to remove valuable signals portion or noise lying in a desired frequency range [1-3]. Two types of filters are there such as analog filter (AF) and digital filter (DF). An AF uses analog electronic circuits made by capacitor, operational amplifier and resisters to produce the essential filtering result [4]. DF uses a digital processor for sampled value of signal to achieve arithmetical calculations.

In Signal processing applications, execution and design of filters is a part of exploration. In the flexible realizations of digital filter and hardware efficient, various research works required in existing DF technique, and it's delivering frequency responses by monitoring a less factors. Unbridged VDFs cut off frequency are wanted for the all pass transformation (APT) technique is known as frequency distorted VDFs [5-11]. The applications are hearing aids, audio equalizer, etc.

Frequency specific filters is the variable digital filters with tunable frequency abilities. Consequently, applying the low-go to low-pass transformation, the transfer function H (z) with mutable qualities can be developed [12]. The coefficients of H (z) are complicated elements of the variable parameter ξ. In this way, they involve an immense number of calculation to tune the coefficients. Linear calculation is required to the coefficients in order to moderate the amount of calculations [13]. Variable digital filters have various potential applications in image processing, communication and acoustic signal processing. In such applications, variable filters are essential to change their coefficients frequently with the final aim that the frequency-domain qualities can be achieved [14].

The All Pass Transformation (APT) based VDFs (APT-VDFs) are developed by displacing of all unit setback to a digital filter. APT construction of appropriate order and they permit on-the-fly command above the cut-off frequency [15]. A low intricacy APT-VDF offers mutable BS, BP, HP and LP responses from a stable coefficient model filter. In any case, on account of non-linear phase characteristic. For model filter design, all pass filter proper arrangements are utilized to restore the delay components [16-17]. 50% filter coefficient is required to reducing the VDF execution intricacy.

This paper proposes design of APT-VDF based on novel RTSD adder and modified booth multiplier technique. In these days, APT-VDF design is challenging for various audio processing applications. Hence, the implementation of high speed APT-VDF with better operational frequency will be the main objectives of many researchers. But, all are concentrating only on the design modification of VDF to increase its presentation. The proposed work planned to design a modified pipeline APT-VPT from arithmetic prospective. So the addition & multiplication are the basic arithmetic operations used to define the convolution equations, they are the purposes of the design investigation. The rest of the paper is arranged in following way; the division 2 define the literature review and major contributions of the APT-VDF. The proposed work is explained in section 3. The fourth section describes the design process of FIR filter in addition result and comparison process is discussed in the section 5. The next section 6 covers the conclusion part for design and implementation APT-VDF using RTSD adder and modified booth multiplier.

2. RELATED WORKS

Some of the latest works interrelated to this paper are given below. Veena and Anju Mohan had suggested variable digital filter based on improved coefficient decimation method. Therefore, the digital front end needs variable digital filters (VDFs) that deliver variable low pass (LP), high-pass (HP), band pass (BP) as well as band stop (BS). CRs and SDR

require multi-standard wireless communication receivers (MWCRs) to integrate prevailing and imminent communication standards into a single generic hardware platform. Variable digital filter established on improved coefficient decimation method gives better performance. The frequency range of the improved coefficient decimation method is very high, that is 179.261MHz.

The different frequency of filter can furnished by complete restraint cut of frequency of fly, lacking filter coefficients were talked about by A. Ambede and A.P.Vinod *et al.*, [20].Here first & second order APT based VDFs alongside equipment execution structures , also propose the altered pipelined equipment's usage models for both the first &second order. Various first &second order field programmable results of both pipelined and non pipelined execution structure were displayed. Suggested execution structure of pipelined fast VDFs results accomplishing with highest working frequencies and independent of filter arranges for both first & second order plans.

Low complexity variable digital filter based on minimal spanning tree application were developed by Elias and Bindima [19]. In this paper had suggested for minimal spanning tree application and multi objective artificial bee colony optimization. Shift comprehensive differential coefficients (SIDCs) and common sub expression elimination (CSE) are organized by minimal spanning of tree method. Hence, the structural design achieves better performance when compared with other existing technique. The frequency range and power consumption of the variable digital filter based on minimal tree application method is 263.995MHz and 4.027W.

3. PROPOSED METHODOLOGY

Variable Digital Filters are most important element in communication and signal processing. Speed and area optimization are the important necessities of APT-VDF design. For multiplication, modified booth encoding is utilized in order to lessen the quantity of partial products. Consequently, considering carry-propagation free addition strategies should improve the addition operation of the filter. Therefore for improving addition speed, consider carry-propagation free addition approaches. The method used to enhance speed of addition utilized in this work is redundant ternary signed-digit (RTSD***)*** number framework. The redundant ternary illustration uses number of bits than the single binary digit. Exceptional behaviour of RTSD supports the calculation along with the lack of classic carry propagation.

Figure 1 represents the proposed design of pipelined APT-VDF at which RTSD adder performs the addition operation and modified version of booth multiplier is used at the place of H (Z) function. At which A1 & A2 are the constant coefficients used for the multiplication purpose. First and second order all pass filter can also be implemented as figure 1 using proposed method. Actually, the usage of RTSD increases the overall design speed due to its carry free propagation. As well as modified booth multiplier reduces the amount of partial product generation as much as possible. It is also one reason for the raise in operational frequency than convention type of pipelined APT-VDF.

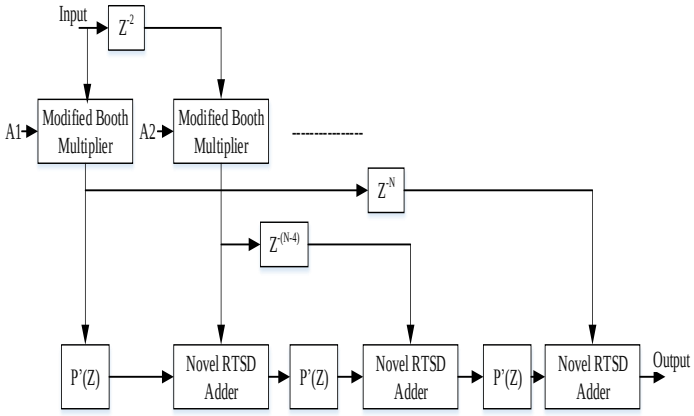

Figure 1: Proposed Architecture of APT-VDF

3.1 Proposed Novel RTSD Adder

The Redundant ternary Number Representation (RTNR) uses more bits and hence every number having lot of representations. Negative values are available in RTNR representation but single sign bit is absent to check if the particular number is positive or negative. The expression $\sum_{k=0}^{n-1} A_k 2^k$ is used to transform redundant ternary representation to integer form. In which, number of digits is represented as n and the deduced value of the k^{th} digit is denoted as A_k . k is the right most location and starts at 0 . The Proposed RTSD enhances the speed of the math operations. The addition with carry propagation done by the proposed RTSD adder. A particular method should be used for the elimination of carry propagation to avoid the issues related with the carry propagation. Here, the addition process of all digits can be performed simultaneously.

$$D_i + F_i = 2g_i + h_i \quad (1)$$

The equation (1) is the fundamental formula for the RTSD arithmetic operation. Where, D_i & F_i are the two operands, the transfer digit (g_i) and interior sum digit (h_i) can be calculated using the table 1 [21].

$$S_i = g_i + h_i \quad (2)$$

The final sum digit (S_i) can be calculated by adding transfer digit and interior sum digit. There is no way to produce a new transfer digit. The steps used for adding two operand is given below:

- In first step the transfer digit is $|g_i| = 1$ only if $|D_i + F_i| \geq 1$

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- In second step the transfer digit $|g_i| = 1$ only if $|g_i + h_i| = 2$ under these conditions both g_i & h_i cannot be 1.
- In third step the final sum bits is calculated by carry fee addition of g_i & h_i

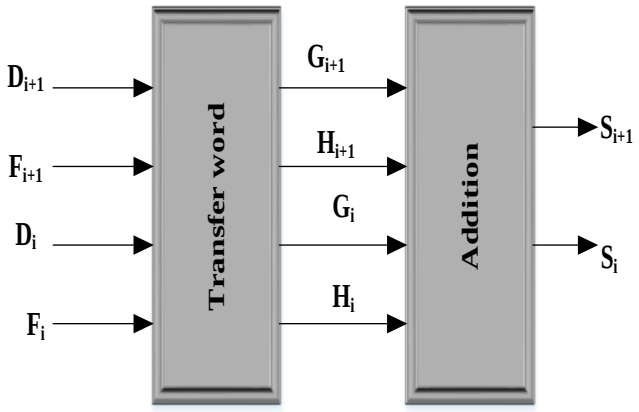


Figure 2: Architecture of RTSD Representation

Figure 2 displays the general block of the proposed RTSD adder. The inputs are D_i & F_i which are given as input to the transfer word block. Where (g_i) represent the transfer digit and (h_i) denotes the interior sum digit .These $g_i and\ h_i$ are the outcomes of the transfer word block. In the above figure, the transfer digit G_{i+1} is assigned to the next addition block to terminate the carry propagation process.

Table 1: interior sum and transfer digit of RTSD [21]

	-2	2	-1	1	-2	2	-1	1	-2	2	-1	1	-4	4	
	X_4	X_3	X_2	X_1	Y_4	Y_3	Y_2	Y_1	Z_4	Z_3	Z_2	Z_1	C_2	C_1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0	0	0	-1
3	0	0	0	0	0	0	1	1	-	-	-	-	-	-	-
4	0	0	0	0	0	1	0	0	0	1	0	0	0	0	2
5	0	0	0	0	0	1	0	1	0	0	1	0	0	1	3
6	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1
7	0	0	0	0	0	1	1	1	-	-	-	-	-	-	-
8	0	0	0	0	1	0	0	0	1	0	0	0	0	0	-2
9	0	0	0	0	1	0	0	1	0	0	0	0	0	0	-1
10	0	0	0	0	1	0	1	0	0	0	1	1	1	0	-3

Algorithm and representation

$$2W_{2i+1} + W_{2i} = [2(X_{2i+1} + Y_{2i+1}) + (X_{2i} + Y_{2i})] - 4t_{2i+2}$$
$$and\ S_i = (W_{2i+1} + W_{2i}) + t_{2i+2}$$

Z	T	t_{2i+2}
1	-3	-1
0	-4	-1
-1	-5	-1
-2	-6	-1
-1	3	1
0	4	1
1	5	1
2	6	1

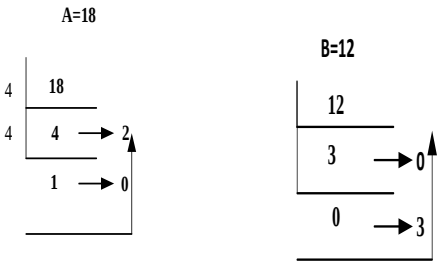
Where,

$$Z = 2W_{2i+1} + W_{2i}\ and\ T = [2(X_{2i+1} + Y_{2i+1}) + (X_{2i} + Y_{2i})]$$

Example: Carry free addition based on RTSD method of (18) & (-12) is given below.

Assume A= (18) & B= (-12)

Step 1: Calculate the Quaternary Signed Digit (QSD) representation of A & B.



$$A \Rightarrow 18 = (102)$$
$$B \Rightarrow -12 = (030)$$

The B value is negative so it's corresponding QSD representation will be $B \Rightarrow (-12) = (0 \quad -3 \quad 0)$.

Step 2: Transform the QSD representation of A & B in terms of binary numbers based on $(-2, +2, -1, +1)$ format.

-2 +2 -1 +1 -2 +2 -1 +1

-2+2-1+1

(1 0 2) = 0 0 0 1 0 0 0 0

0 1 0 0

(0 -3 0) = 0 0 0 0 1 0 1 0

0 0 0 0

---

0 1

2

In the above addition of A & B, add the resultant bit values from $(-2,+2,-1,+1)$ for the presence of 1 in the binary representation. If sum digit is above 2 or -2, then the take carry bit, e.g. if sum digit is -3 then take -3= -2 -1, so final sum is +1 and carry (-1) move to next MSB.

Step 3: Finally add the resultant values (0 1 2) as follows

(0 1

2)= $(0\times4^2+1\times4^1+2\times4^0)$

= 4+2

= 6

After the completion of binary addition, the value will be converted into decimal value. Delay enhancement, highly efficient, carry free addition and independency of word length are selected advantages of RTSD adder.

3.2 Proposed modified booth multiplier

The multiplication process includes three steps like addition partial product generation and partial product elimination. The modified booth algorithm are used to perform a high speed multiplication process. Figure 3 shows the architecture of modified booth multiplier. The final step addition gives the final product of modified booth multiplier. Table 1 represents the radix-4 booth recoding table.

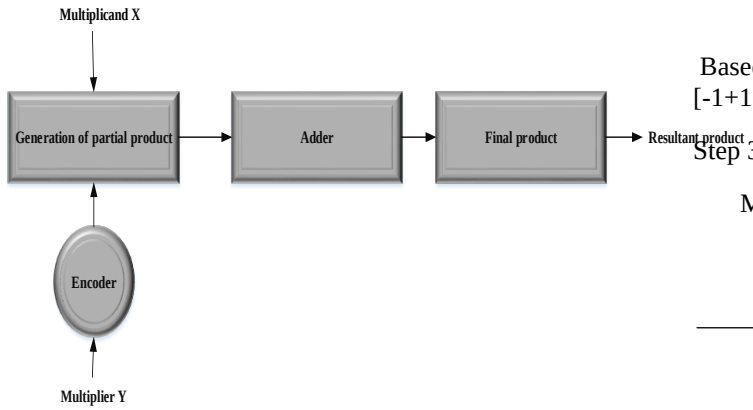


Figure 3: Architecture of modified booth multiplier

Table 2: Radix-4 booth recoding table

Multiplier bit pair		Multiplier bit on the right	Recoded multiplier in booth's algorithm		Bit pair recoded multiplier bit at position
i+1	i	i-1	i+1	i	i
0	0	0	0	0	0
0	0	1	0	+1	+1
0	1	0	+1	-1	+1
0	1	1	+1	0	+2
1	0	0	-1	0	-2
1	0	1	-1	+1	-1
1	1	0	0	-1	-1
1	1	1	0	0	0

Modified booth multiplier can be expressed in below equation

$$Zj = q2j + q2j-1 - 2q2j+1 \text{ with } q-1 = 0 \quad (3)$$

Example: Multiplication of two numbers (12) & (-6) is given below,

Step 1: Find the binary representation of (12) & (-6)

Multiplicand 12 =01100

Multiplier +6 =0110

Multiplier -6=11010(take 2'complement of 0110)

The multiplicand and multiplier value is positive means, it will add 0's at leftmost position otherwise it will add 1's at leftmost position.

Step 2: Find the booth recoding and bit pair recoding

Multiplier = $\overline{1}\ 1\ \overline{0}\ 1\ \overline{0}\ 0$ (add extra bit 0's at right position)

Booth recoding = $0\quad 0\quad -1\quad +1\quad -1\quad 0$

= [0 0] [-1 +1] [-1 0]

Bit pair recoding= $0\quad -1\quad -2$

Based on the radix 4 booth recoding table, the value [0 0], [-1+1] and [-1 0] can be written as 0 -1 and -2.

Step 3: Finally the resultant values (12) & (-6) as follows

Multiplicand → 1 1 0 1 0 0

0 -1 -2

---

1 1 1 1 1 0 1 0 0 0

1 1 1 1 0 1 0 0

0 0 0 0 0 0

1 1 1 0 1 1 1 0 0 0

The multiplier value is [0 -1 -2] , take 2's complement multiplicand, if value is -1 and -2 means take 2's complement multiplicand in two times. Leftmost position 1 denotes the negative value. So, the final answer will be the negative value. Take 2's complement of 1 1 0 1 1 1 0 0 0.

2's complement of 1 1 0 1 1 1 0 0 0 = 0 0 1 0 0 1 0 0 0

Finally add the resultant values (0 0 1 0 0 1 0 0 0) as follows,

$$(0\,0\,1\,0\,0\,1\,0\,0\,0) = -[(0\times 256)+(0\times 128)+(1\times 64)+(0\times 3\ldots\times 16)+\ldots+(0\times 2\ldots)]$$
$$= -[(64)+(8)]$$
$$= (-72)$$

After the completion of binary addition, the value will be converted into decimal value. Finally the resultant value is – 72.

4. FIR Filter Design

Digital filtering is an essential block for the continual development in digital signal processing (DSP) applications. Digital filtering technique is regularly used for the particular frequency attenuation, enhancing signal strength, noise suppression and various specific operations. The digital filter designs are classified into two types. There are FIR (Finite Impulse Response) and IIR (Infinite impulse Response).

The FIR filter is designed by the APT-VDF design technique. The FIR filter main components is delay, multiplier and adder .The figure 3 demonstrates the structure of FIR filter. The carry propagation delay is main limiting factor for adder and multiplier. The latency of the finite impulse response filter is reduced by using a redundant number based improved booth multiplier, and new RTSD adder. The basic equation of the filters impulse response can be considered for the purpose of implementation.

$$b[n] = \sum_{\lambda=0}^{n} S(\lambda)a[n-\lambda] \quad (4)$$

Where, a[n] and b[n] denotes the input and output port of FIR filter. Therefore, modified booth multiplier is used for speedup performance and decreases the area. This multiplier block achieve the function of the modified booth multiplier that is clearly explained in the division 3.2. The RTSD adder perform the addition operation as described in the part 3.1.The presentation of the finite impulse response is generally affected by the slow working of multiplier device. The inversion and shift in the $a[n]$ are represented by the delay. The delay block is multiplied by the constant coefficient value S. Hence, corresponding coefficient and new data sample are given as inputs to the multiplier. This suggested work uses the RTSD adder and it is adds the negative and positive parts of signed digit number. The final result of the FIR filter is delay free outcome with developed less complexity and parallelism.

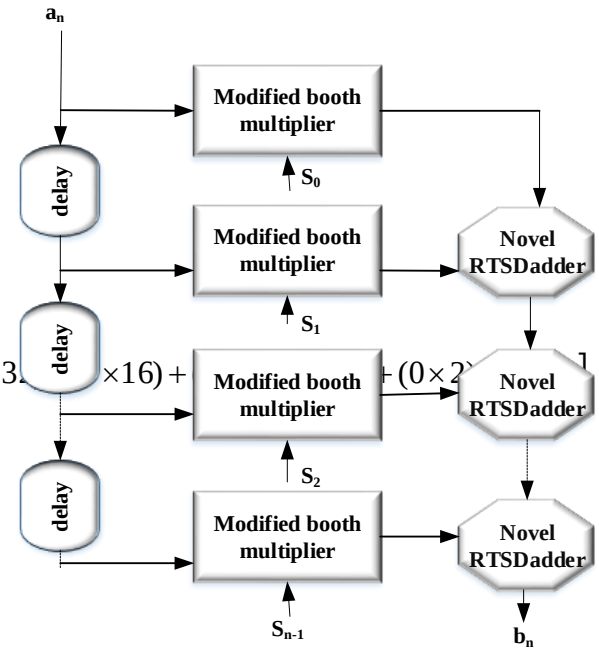
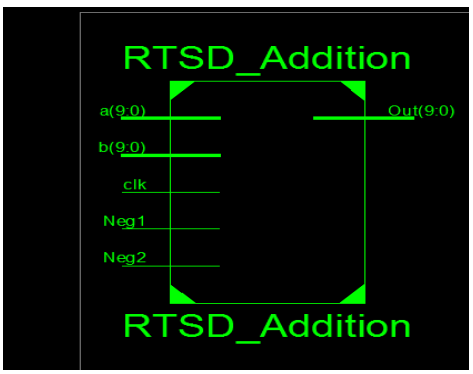


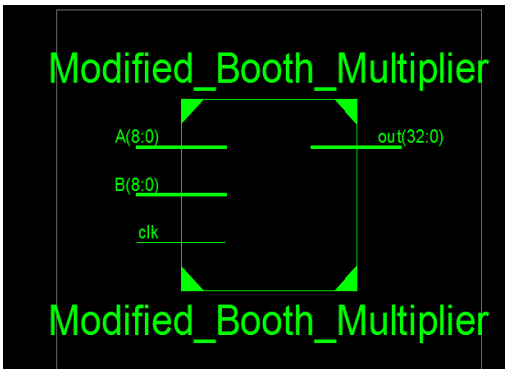
Figure 4: Structure of FIR filter

5. Result and Discussion

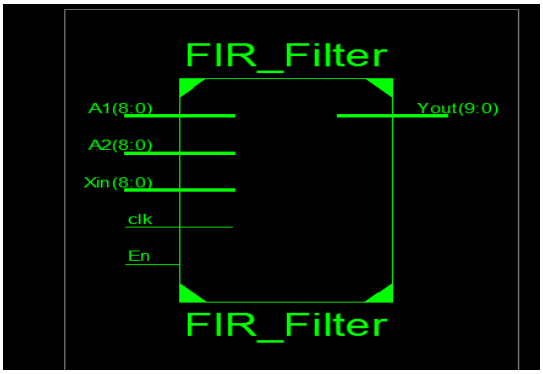
The implementation of APT-VDF using novel RTSD adder and modified booth multiplier performed in Verilog on structural Register Transfer Level (RTL). The Xilinx ISE 14.5 tool is used for simulation and synthesis of planned APT-VDF. The suggested work containing RTSD adder, modified booth multiplier and FIR filter. The RTL view of RTSD adder and modified booth multiplier is shown in figure 5 (a) and 5 (b). The figure 5 (c) shows the RTL view of proposed FIR filter. The APT-VDF was designed in Virtex6xc6v.

a) RTSD adder





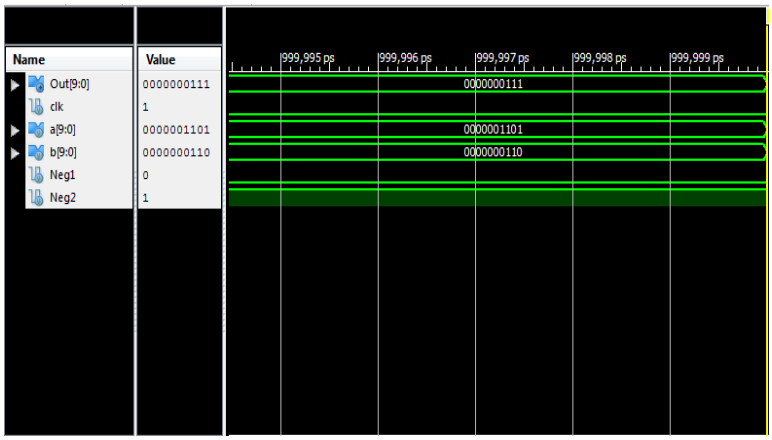
b) modified booth multiplier



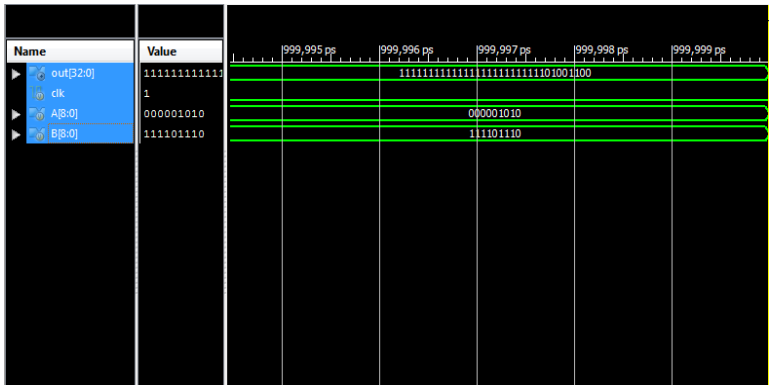
c) FIR filter

Figure 5: RTL view of proposed work

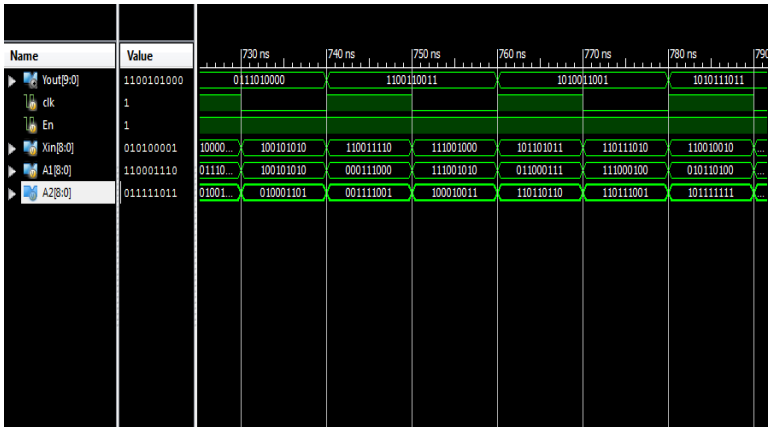
Figure 6: shows the simulation results of the work for (5a) RTSD adder, (5b) modified booth modifier and (5c) FIR filter. Similarly, the device utilization of the proposed work is taken through the Xilinx implementation of filter blocks. The two values like (13) & (-6) are taken for the implementation purpose of RTSD adder as an example. In figure (5a), the two inputs are 0 0 0 0 0 0 1 1 0 1 & 0 0 0 0 0 0 0 0 1 1 0 and the equivalent carry free result will be 0 0 0 0 0 0 0 1 1 1. Here, Neg 2 value is assigned as 1 to indicate the negative part of one of the inputs. In figure (5b), the values of 10 & (-12) are considered for the implementation of modified booth multiplier. Similarly, the implementation of FIR filter is shown in the figure (5c).



a) RTSD adder



b) modified booth multiplier



c) FIR filter

Figure 6: Simulation result of proposed work

The figure 7 displays the device utilization of proposed work. The design summary is measured by the Xilinx device utilization logic implementation report. The below tabular represents the comparison of components utilization from the available components. The device utilization table contains number of slice registers; look up tables (LUTs), flip-flops, input/output components and slices. From the adder design using RTSD number system

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	850	687360	0%
Number of Slice LUTs	799	343680	0%
Number of fully used LUT-FF pairs	560	1089	51%
Number of bonded IOBs	38	1200	3%
Number of BUFG/BUFGCTRL/BUFHCEs	1	248	0%

Figure 7: device utilization of proposed work

APT-VDF design using RTSD adder and modified booth multiplier is compared with various existing technique. The various existing methods are: design of variable digital filter based on Improved Coefficient Decimation Method (ICDM) [18], design of low complexity variable digital filter using minimal spanning tree application [19], design of high speed APT based VDF [20].Compared with existing technique , the proposed work gives better operational frequency and power consumption. Existing techniques are compared with proposed APT-VDF and displayed in table 2.

Table 2: Comparison of proposed work with existing technique

Resources	Reference 18	Reference 19	Reference 20	Proposed
Flip-Flops	633	628	607	560
Number of LUT's	867	842	811	799
Number of slices	978	918	893	850
Number of IOB's	79	71	64	38
Operating frequency(MHz)	179.261 MHz	263.995 MHz	305.153 MHz	325.119 MHz
Power consumption(W)	4.143	4.027	3.982	3.769
Latency(ns)	3.172	3.151	3.098	3.076

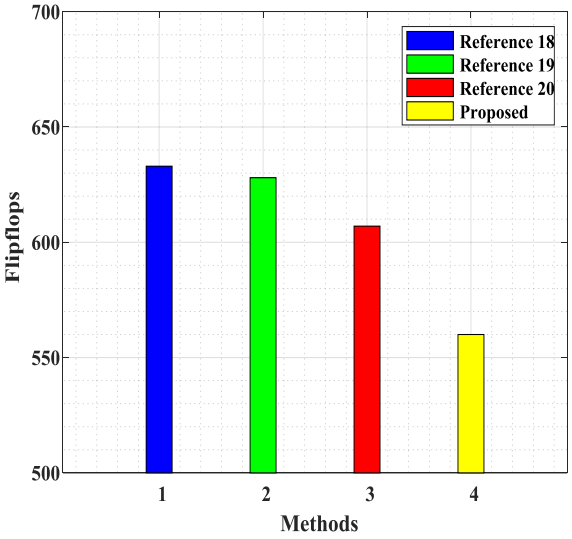


Figure 8: Comparison analysis of Flip Flops

Compared with various existing technique, the proposed work have less number of flip flops. The number of flip flops in reference 18, 19 and 20 is 633, 628 and 607. In our proposed method approach the flip flops is 560.Figure 8 shows the comparison analysis of flip flops.

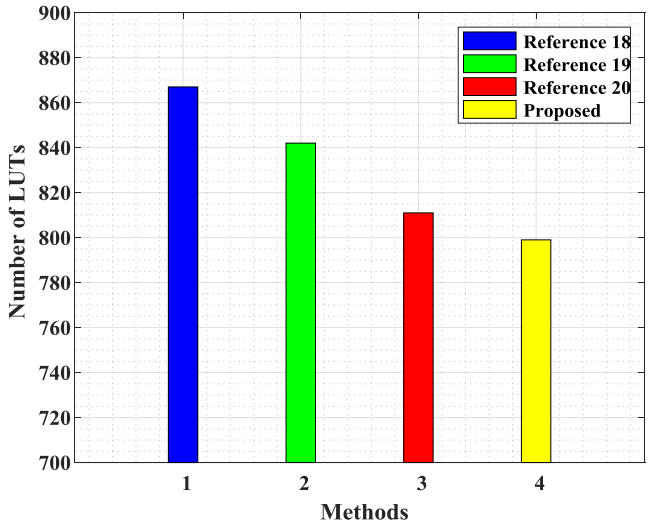


Figure 9: Comparison analysis of LUTs

Figure 9 shows the number of LUTs comparison with various existing technique. The proposed design and implementation of APT-VDF achieves the number of LUTs is 799 in addition the LUTs values of existing technique include reference 18 (867), reference 19(842) and reference 20 (811).

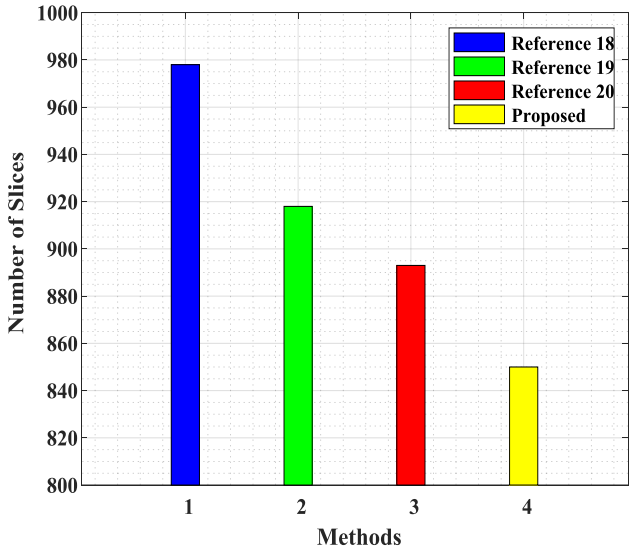


Figure 10: Comparison analysis of slices

Figure 10 illustrate the comparison analysis of slices. Proposed method achieves the number of slices 850 in addition the number of slices in existing technique contain reference 18 (978), reference 19 (918) and reference 20 (893).

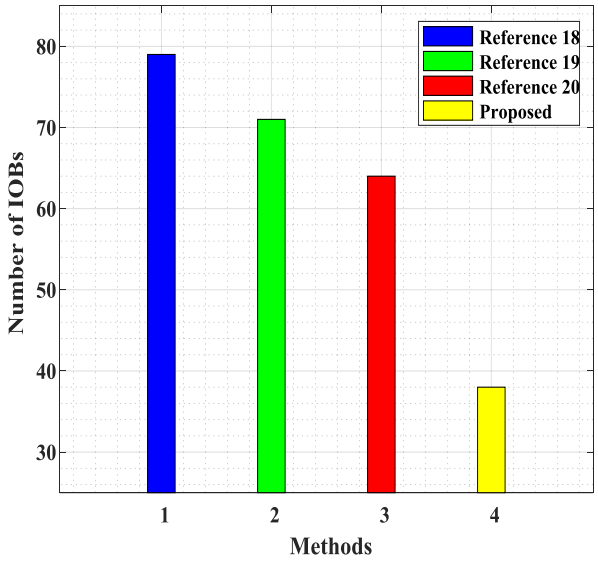


Figure 11: Comparison analysis of IOB'S

Figure 11 represent the comparison analysis of IOB's. The number of IOB's in existing technique include reference 18 (79), reference 19 (71), and reference 20 (64). The proposed method achieves the number of IOB's is 38.

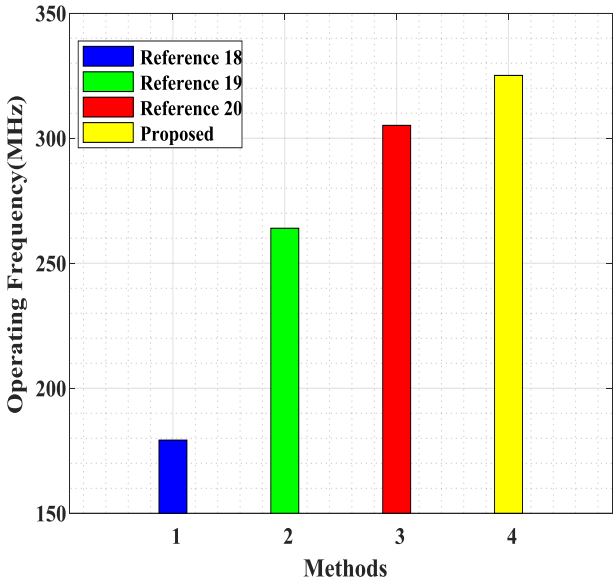


Figure 12: Comparison analysis of frequency

Figure 12 shows the frequency comparison with various existing technique. The proposed design and implementation of APT-VDF achieves the frequency range is 325.119MHz in addition the frequency range of existing technique include reference 18 (179.261 MHz), reference 19 (263.995 MHz), reference 20 (305.153MHz).

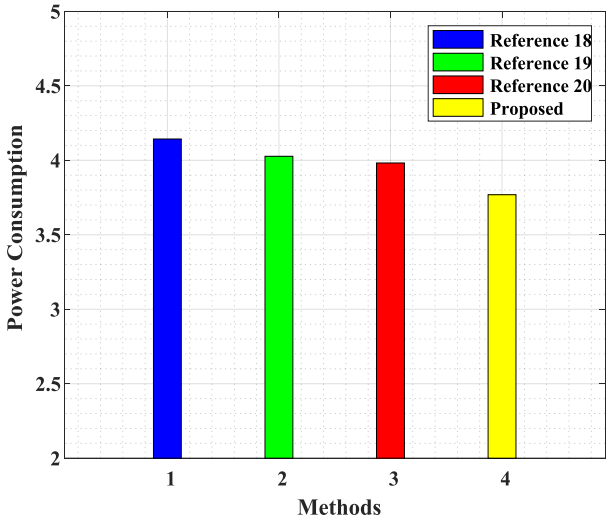


Figure 13: Comparison analysis of power consumption

Figure 13 demonstrate the power consumption comparison with other existing technique. The proposed APT-VDF design consumes power value of 3.769W also the power consumption values of existing technique contain reference 18 (4.143W), reference 19 (4.027 W), reference 20 (3.982W).

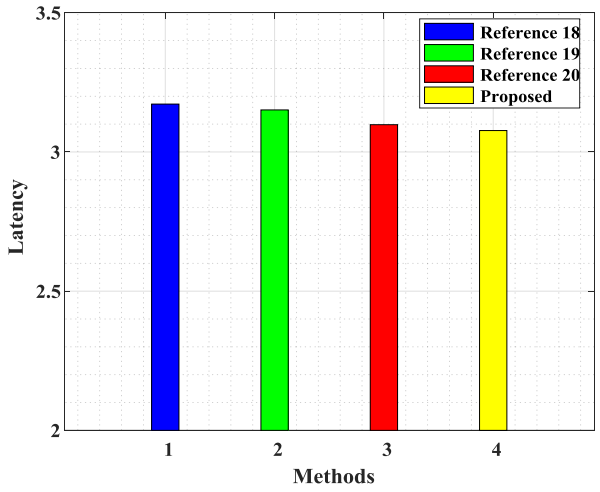


Figure 14: Comparison analysis of latency

Fig 14 shows the latency contrasted with various existing techniques. The proposed APT-VDF design achieves the latency value is 3.076ns additionally the latency values of the existing techniques include reference18 (3.172ns), reference 19 (3.151ns), reference 20 (3.098).

6 Conclusion

In this work, VLSI design and implementation of APT-VDF using RTSD adder and modified booth multiplier have been approached from the arithmetic perspective. There is no carry propagation after the second stage of addition in the adder architecture employing the RTSD number system. As a result, the length of the maximum carry propagation chain will be reduced, reducing the time required for addition. The APT-VDF was designed in Virtex6 xc6v. Xilinx ISE design suite 14.5 is used for the simulation and synthesis of proposed scheme. The scheme of APT-VDF occupies less power, less area and high speed. The proposed APT-VDF design is synthesised using Xilinx tool and compared the results with existing methods in terms of 799 flip flops, 850 slices, 38 IOB's, 325.119(MHz) operating frequency, 3.769(W) power consumption and 3.076 (ns) latency. To get better development for APT-VDF design using new optimization technique in future.

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