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# A Novel Asymmetrical Multilevel Inverter for Higher Output Voltage Levels

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***Abstract— In this Paper focus on design and achievement of the new topology in a multilevel inverter with a reduction harmonic, size, cost in higher efficiency the main objective of this work a novel three-phase inverter with applicable in induction motor drive in medium voltage application. The main advantage of the new topology is to reduce the THD (Total Harmonic Distortion) lower electromagnetic interference generation and higher output voltage for applicable induction motor drive.This work describes a reduce harmonic in a single phase seven level, Twenty level & Twenty seven level inverter circuit with new level shift pulse width modulation (LSPWM) scheme is purposed. This topology is a combination of a threesingle level full bridge inverter circuit. There are many topologies of multilevel inverters in literature, popular among them are cascaded H-bridge. In general the control methods of these cascaded inverters are designed an assumption of having all dc source voltages same for all H-bridges. The performance of the purposed a novel seven, twenty three, and twenty seven level multilevel inverter with same number of H-bridges is modified with the inherent benefits & isolated DC sources, The multilevel carrier based Level shifted pulse width modulation methods are used in this topology a seven, twenty three, and twenty seven level output voltage wave forms is shown in FFT window. MATLABE/SIMULINK is used to simulate the inverter circuit operation and control signals.***

***Index Terms—Two Level Inverter, Reduced Switches and Sources, Pulse Width Modulation (PWM), Multi Level Inverters.***

## I. INTRODUCTION

The voltage cause inverters create a voltage or a current with levels also 0 or ±V dc they are well-known as two level inverters. They require high switching frequency along with various pulse width modulation (PWM) strategies to get a quality output voltage or a current waveform with a minimum amount of wave content, Surrounded by high power and high voltage application, these two stage inverters, on the other hand, have some restrictions in operating at high frequency mainly due to switching devices should be used in such a way as to keep away from problems connected with their series-parallel combinations that are necessary to obtain capability of handling high voltages and currents.

The multilevel inverter [MLI] is a shows potential inverter topology for high voltage and high power applications. This inverter synthesizes numerous different levels of DC voltages to produce a staircase with the purpose of approaches the cleansine waveform. It has high power superiority waveforms, lower voltage ratings of devices, lower harmonic deformation, lower switching frequency and switching losses, higher efficiency, and reduction of dt/dv stresses. It gives the possibility of working with low speed semiconductors but its comparison with the two-level inverter. several of MLI topologies and modulation techniques have been introduced and studied comprehensively. But most accepted MLI topologies are Cascaded Multilevel Inverter (CMLI), Diode Clamp and Flying Capacitor. In this thesis we employ a CMLI that consist of some with not the same DC named as Asymmetric Cascaded Multilevel Inverter (ACMLI) and H-Bridge inverters. It is implemented because these inverters are more modular and simple in creation and have other reward than flying capacitor and Diode clamp.

## II. TYPES OF MULTI-LEVEL INVERTERS

Multilevel inverter is very versatile and is uses for power electronics topology for high power application. The multilevel inverter has a very low electromagnetic interference (EMI),The voltage across the switches is only one half of the DC source voltage, The switching frequency can be reduced for the same switching losses, The higher output current harmonics are reduced by the same switching frequency. It efficiency is high compare to conventional inverter. Multilevel inverter is a most recentoption to execute low frequency based inverters with low output voltage twist. Basic multilevel topologies are of three types.: 1. Diode-Clamped Multilevel Inverter 2 .Capacitor Clamped/Flying Capacitor Inverter 3. Cascade H-bridge (CHB)

Every three topologies of a multilevel inverter can be used in reactive power compensation not including having the voltage unbalance problem. Diode clamping is not ideal in fast capacitor and cascaded inverter design and balancing capacitors are not required in diode clamped and cascaded inverter configuration. In cascaded inverter configuration requires the smallest amount number of components.

The diode clamped topology is also called as a neutral point converter. It was the first widely popular multilevel inverter topology. It is comprehensively used in industrial application this three levels neutral point converter uses capacitor to generate intermediate voltage level and voltages across the switches are only half cycle in dc input. These inverters most commonly used in medium power and high power voltages. In this inverter topology diode is used as the clamping device to clamp the dc bus voltage so the same as to achieve steps in the output voltage. Thus, the major concept of this inverter is to use diodes to bind the power devices voltage stress. The voltage over each capacitor and each switch is Vdc.

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A similar topology to the Neutral-Point Clamped Multilevel Inverter topology is the Capacitor Clamped (CC), or FlyingCapacitor, multilevel inverter topology, As a substitute of using clamping diodes it use capacitors to hold the voltages to the desired values. As for the Neutral-Point Clamped Multilevel Inverter,(m-1) number of capacitors on a shared DC-bus, where m is the level number of the inverter, and 2(m-1) switch-diode valve pairs are used. On the other hand, for the CCMLI, instead of clamping diodes, one or more (depending on position and level of the inverter) capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position on each side of the midpoint between the valves [3].

**Cascade H-bridge (CHB):** configuration has newly happen to very popular in adjustable-speed drive and high-power AC supplies applications. In each of its three phases, cascade multilevel inverter contains of a series of H-bridge (single-phase full bridge) inverter units. Each one H-bridge unit has its personal DC source, which for an induction motor would be a battery unit, solar cell or fuel cell.

## III. PROPOSED TOPOLOGY

The graphic arrangement of the proposedblock Diagram of Multi Level inverter is shown in figure -3.1. The DC-link is universal for all the phases. Each phase consists of a three-level arrangement connected to common DC-link and a full-bridge with FC coupled at the output of three-level arrangement.

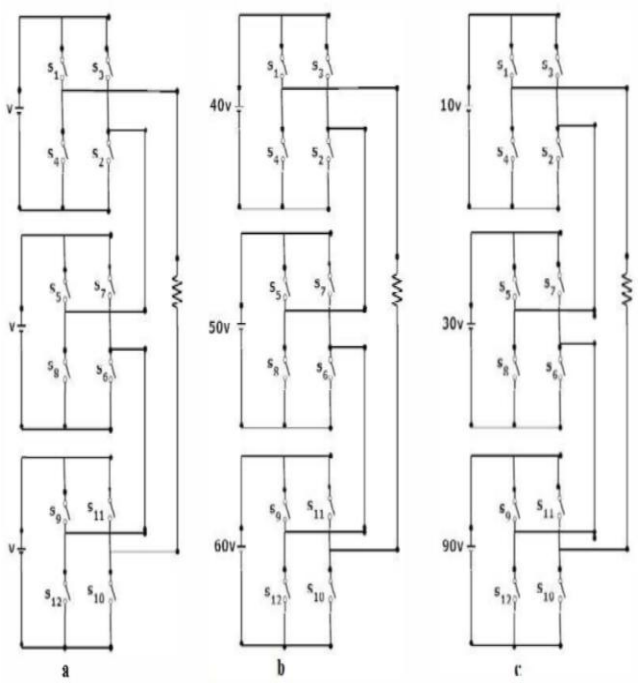


**Figure-3.1** Proposed block diagram

Each D.C. source is connected with a single-phase full-bridge inverter. The AC terminal voltages of different level inverters are linked in series. Each one converter level can generate three dissimilar voltage outputs, +*Vdc*, -*Vdc*and zero because of dissimilar combinations of the four switches, S1, S2, S3 and S4. The AC outputs of dissimilar full-bridge converters in the identical phase are attached in series such that the synthesized voltage waveform is the addition of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two earlier converters (i.e. diode clamped and flying capacitor). The number of output-phase voltage levels is formulated by *m*= 2N+1, where *N* is the number of DC sources in this topology. A seven-level cascaded converter such that, contents ofthree full bridge converters andthree DC sources. Minimum harmonic deformation can be obtained by controlling the conducting angles on different converter levels. Each H-bridge part generates a quasi-square waveform by phase changing its negative and positive phase legs switching timings. Each switching device for all time conducts 180° (or half cycle) apart from the pulse width of the quasi-square wave. All of the switching devices current stress equal because of this switching method. In the motoring manner, power flows from the batteries from side to side the cascade inverters to the motor.

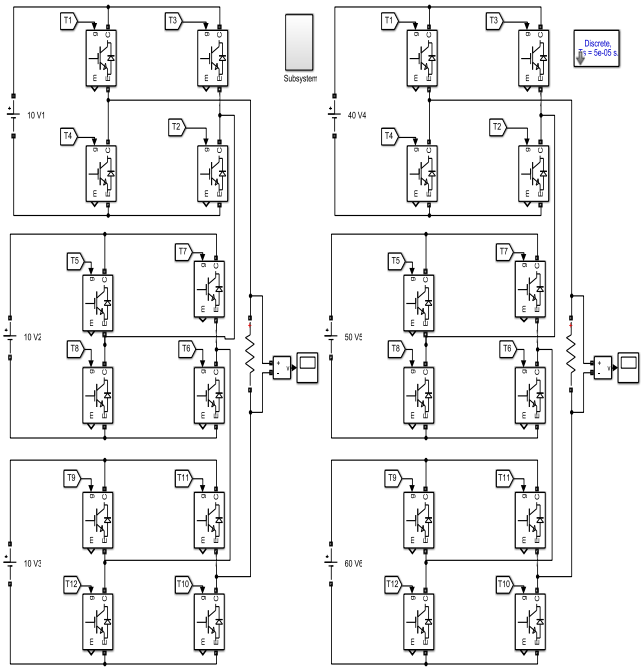

**Figure-3.2** Single Phase Seven-level &Twenty three level H-bridge MLI simulation diagram

The single phase seven level hybrids cascaded multilevel inverter diagram is given Figure 3.2 .this type of the inverter has two types: first one is H-bridge inverter and other is conventional inverter.

The conventional inverter is acting the main inverter and H-bridge inverter is acting the auxiliary inverter.The Main inverter output voltage is either +Vdc/2 (S1isON) or -Vdc/2 (S2 is ON).its connected in series with a full H-bridge that in turn is supplied by a capacitor voltage. If the capacitor is kept charged to Vdc/2, then the output voltage of the H-bridge can take on the values +Vdc/2 (Sa3 &Sa6 ON ), 0 (Sa3,Sa4,Sa5,Sa6 are ON) or -Vdc/2 (Sa4 & Sa5 ON).

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**Table-3.1** Switching States of Seven-Level Inverter

TABLE I. SWITCHING SEQUENCE OF 23-LEVEL CHB INVERTER

| Switches / Voltage Levels | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $2V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| $3V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $4V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $5V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| $6V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| $7V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $9V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| $10V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| $11V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $15V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $0V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $-V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $-2V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $-3V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $-4V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $-5V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| $-6V_{dc}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $-7V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $-9V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| $-10V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| $-11V_{dc}$ | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $-15V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

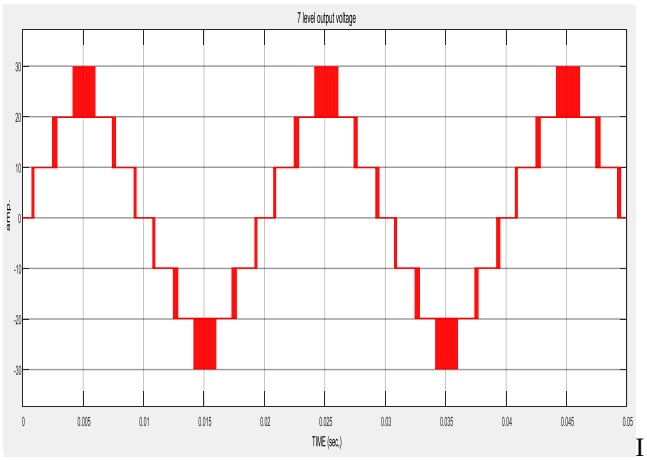
**Table-3.2** Conducting switches at different levels of output voltage

TABLE II. SWITCHING SEQUNCE OF 27-LEVEL CHB INVERTER

| Switches / Voltage Levels | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $2V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $3V_{dc}$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $4V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| $5V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $6V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $7V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $8V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $9V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $10V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| $11V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $12V_{dc}$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $13V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $0V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $-V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $-2V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| $-3V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| $-4V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| $-5V_{dc}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $-6V_{dc}$ | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $-7V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| $-8V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| $-9V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| $-10V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| $-11V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $-12V_{dc}$ | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| $-13V_{dc}$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

Table-3.1 shows the current orders for different operating modes of seven-level& twenty three level inverter.Generation of pulse width modulation signal formula shown in tabel-3.1 these pulses are given for 24 switches use. In this inverter has 12 switches "Sa1, Sa2, Sa3, Sa4, Sb1, Sb2, Sb3, Sb4Sc1, Sc2, Sc3, Sc4 " for upper lag and 12 switches " Sa11, Sa21, Sa31, Sa41 , Sb11, Sb21, Sb31, Sb41 ,Sc11, Sc21, Sc31, Sc41 for lower lag . The corresponding conducting switches and inverter output voltage levels are given in Table 3.2. It can be understand that the number of conducting switches for each level is very less. This ensures the higher efficiency of the proposed seven-level inverter**.**

## IV. SIMULATIONRESULTS




I

**Figure 4.1** output voltage waveform of seven levels MLI

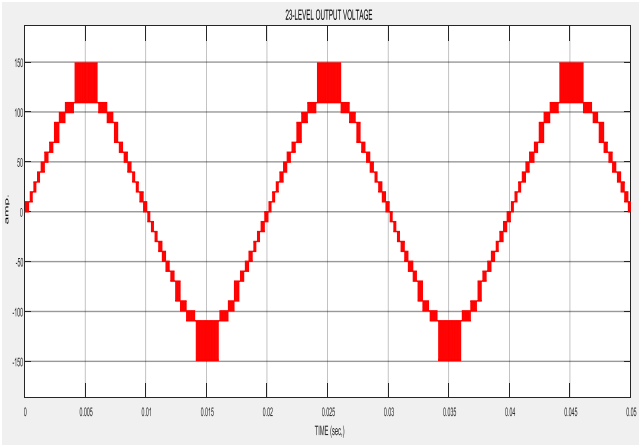



**Figure 4.2** output voltage waveform of twenty three levels MLI

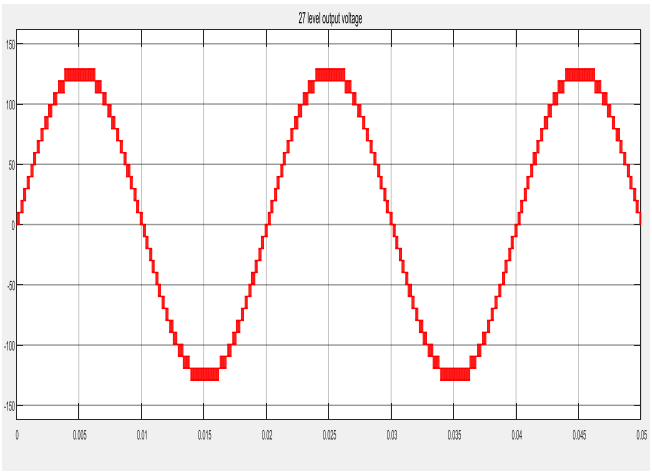



**Figure 4.3** output voltage waveform of twenty seven levels MLI

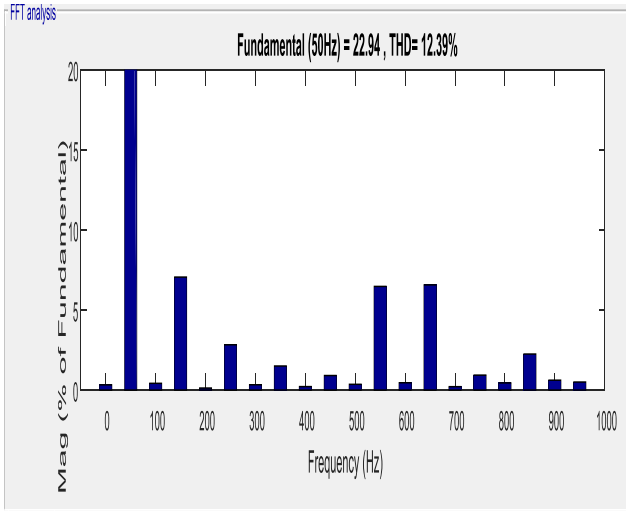



**Figure 4.4** FFT analysis of New seven levels MLI output voltage waveform.

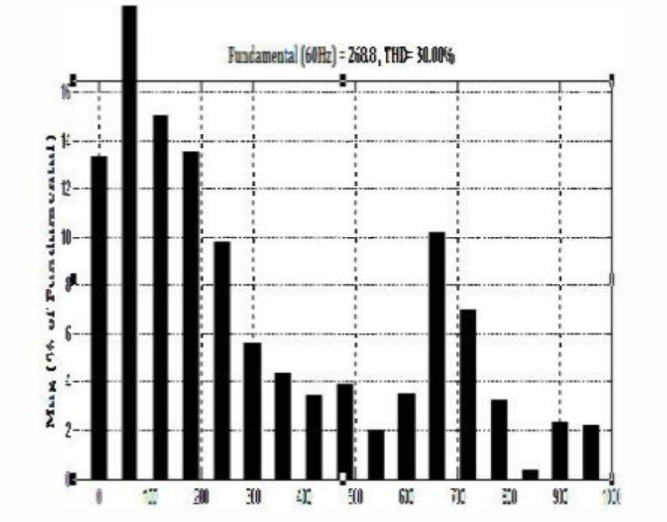



**Figure 4.5** FFT analysis of Old seven levels MLI output voltage waveform.

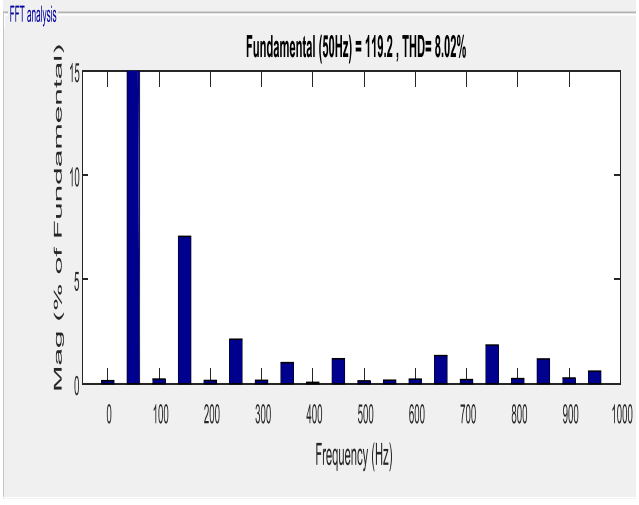



**Figure 4.6** FFT analysis of New Twenty three levels MLI output voltage waveform.

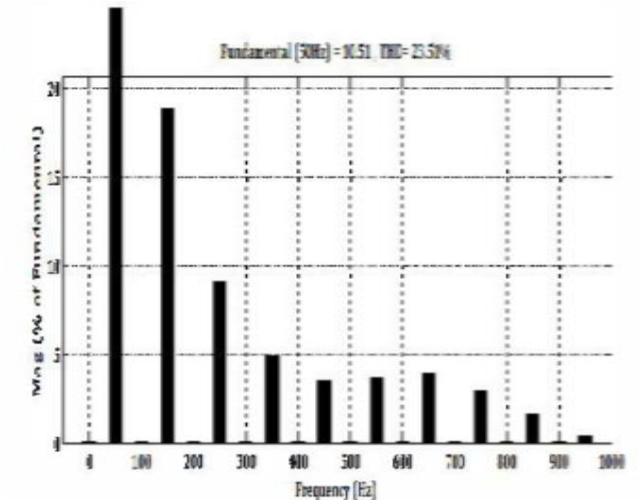


**Figure 4.7** FFT analysis of Old Twenty three levels MLI output voltage waveform.

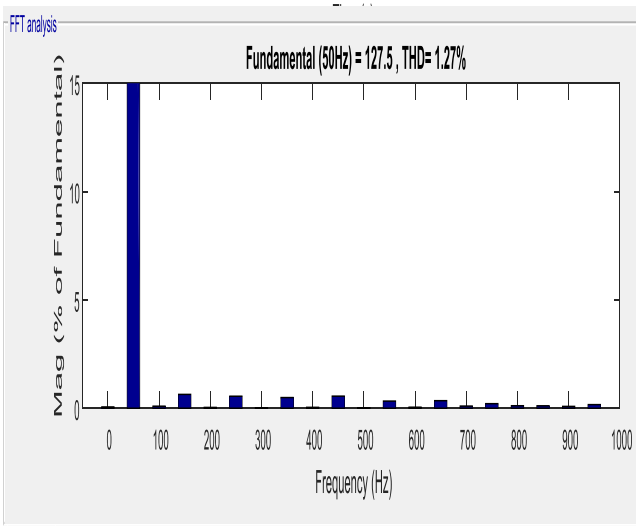



**Figure 4.8** FFT analysis of New Twenty Seven levels MLI output voltage waveform.

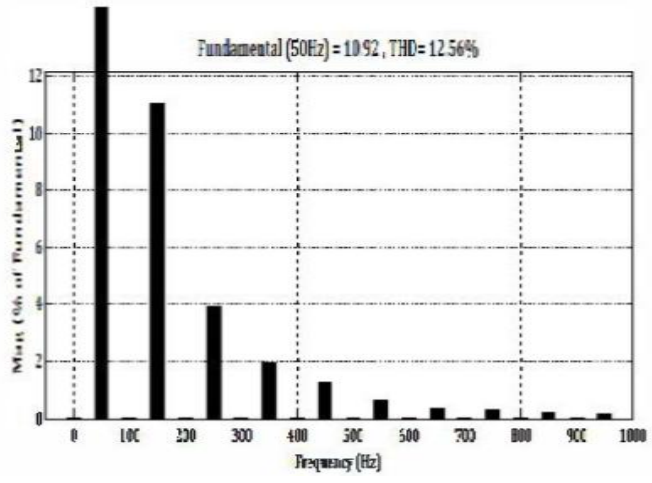



**Figure 4.8** FFT analysis of Old Twenty Seven levels MLI output voltage waveform.

## V. PERFORMANCE ANALYSIS OF SEVEN LEVEL MLI WITH MOTOR LOAD IN PHASE-A

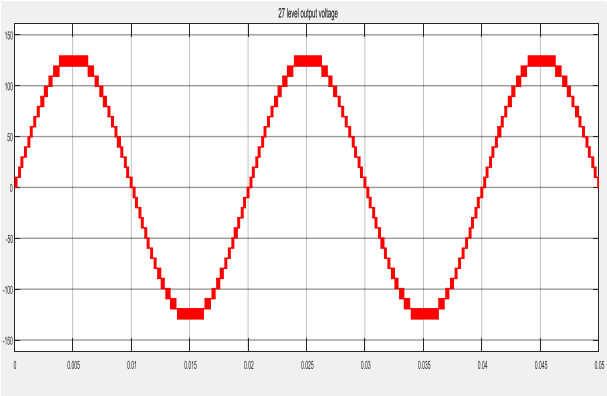



**Figure 5.1** output voltage waveform of twenty seven levels MLI with Induction Motor Load fed.

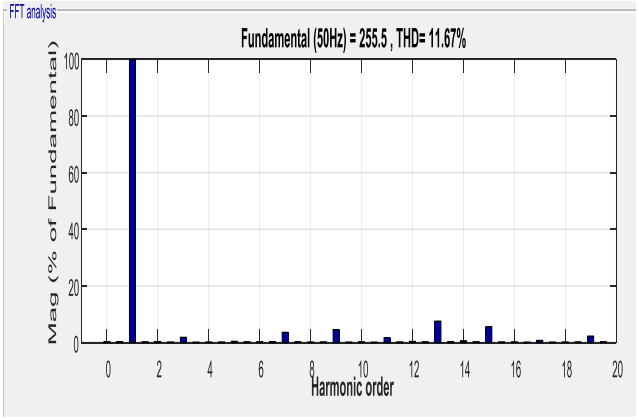



**Figure-5.2** FFT analysis for Oldtwenty seven levels MLI with Induction Motor Load fed.

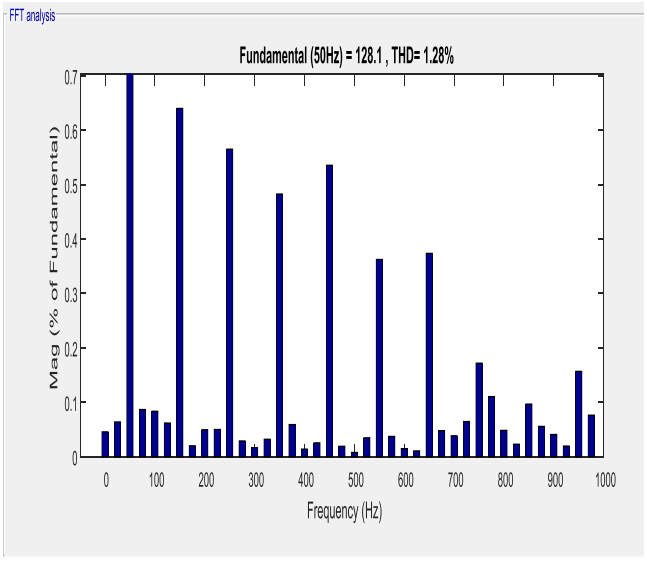



**Figure-5.3** FFT analysis for New twenty seven levels MLI with Induction Motor Load fed.

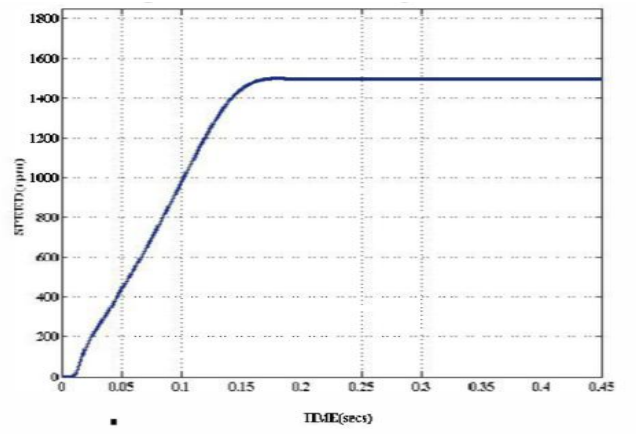



**Figure-5.4** Speed characteristics of old (base paper) for MLI fed induction motor load.

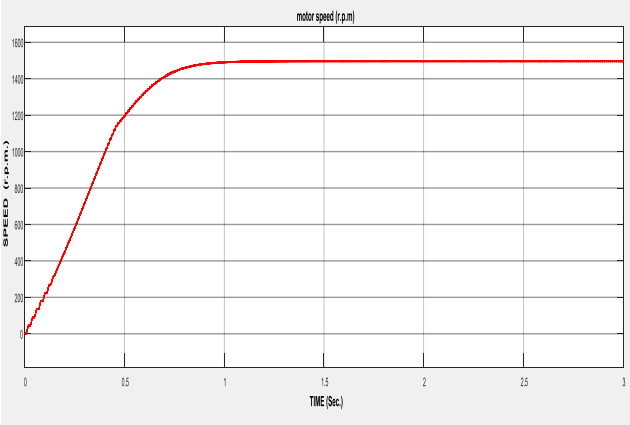



Figure-5.5 Speed characteristics of New MLI fed induction motor load.

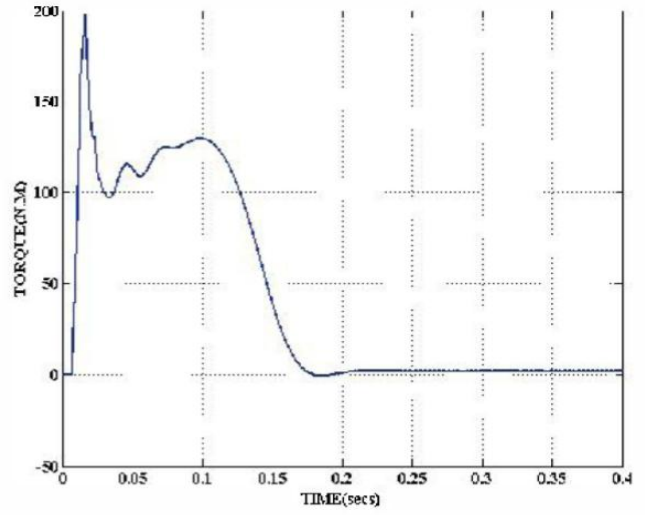



**Figure-5.6** Torque characteristics of old (base paper) for MLI fed induction motor load.

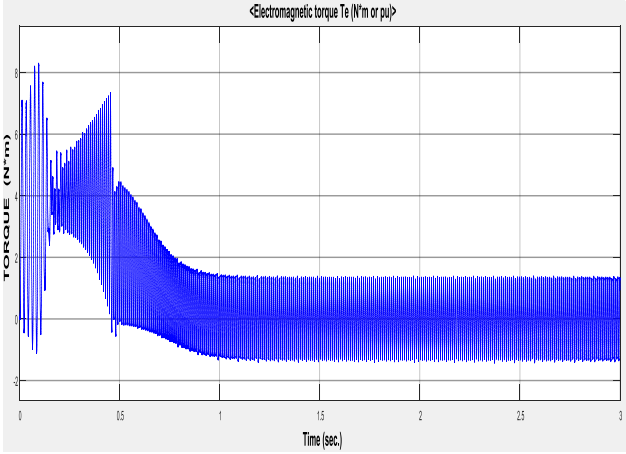



**Figure-5.7** Torque characteristics of New MLI fed induction motor load.

Proposed H-bridge cascaded multilevel inverter circuit. The topology of an inverter circuit is based on the requirement and range.All topologies have both advantages and is advantages. The two level inverters cost is very low as compared to other conventional inverter topologies. but very high value of THD. Then to reduce THD levels of a inverter voltage waveforms should be increased. And the number of level increases in a inverter then switching losses increased. Theses all above problems can be avoided by hybrid multilevel inverter.
Figure-5.2 & Fig.-5.3 Shows in New & Old (Base paper) THD (total harmonics distortion) value for a proposed 3-Phase H-bridge cascaded multilevel inverter circuit with induction motor load in a seven level. This proposed circuit has THD-11.67% for a seven level output voltage waveform.The topology of an inverter circuit is based on the requirement and range.Figure 5.7 Speed Torque Characteristics of 3-phase IM for a proposed H-bridge cascaded multilevel inverter circuit in a seven level. Fig,-4.7 shows proposed circuit THD-11.67% & fig-4.8 shows old (base paper) circuits THD-24.57% for a seven level output voltage waveform.

## V. CONCLUSION

This Paper work has provided a brief summary of implementation 7, 23 & 27- level multilevel inverter circuit is proposed for more improved output as per the requirement. In this proposed circuit output value of the voltage & THD are minor differences with motor load or without motor load shown Table-6.2. Then also the power quality is improved & converter is large stable. Comparison a (Base paper) Old & New MLI without motor load results in 7, 23, & 27 levels HMLI shown in Table-6.1,

**Table: 6.1** Comparison a (Base paper) Old & New MLI without motor load results in 7, 23, & 27 levels HMLI

| HML INVERTERS | THD (Total harmonics distortion) | Fundamental Vol, (50 Hz)= |
|---|---|---|
| **Without motor load** | 1.27 % | 127.5 V. |
| **With motor load** | 1.28 % | 128.1 v. |

**Table: 6.2** Comparison a Result With motor load & Without motor load of New HMLI

| H-BRIDGE INVERTERS | OLD (Base paper)THD (Total harmonics distortion) | NEW (proposed work) THD (Total harmonics distortion) | OLD (Base paper) Fundamental Vol, (50 Hz)= | NEW (proposed work) Fundamental Vol, (50 Hz)= |
|---|---|---|---|---|
| **7-level** | **30.07%** | **12.39 %** | **20.88 V.** | **22.94 V.** |
| **23-level** | **23.5 %** | **8.02 %** | **90.51 V.** | **119.2 V.** |
| **27-level** | **12.56 %** | **1.72 %** | **109.2 V.** | **127.5 V** |

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